F-111D Computer Complex

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A concise description of the Mark II computer complex in the F-111D avionic system is presented. Emphasis is placed on the features related to the computer complex design concept and to the achievement of the design objectives. Operation of the equipment under stored program control is described to illustrate how the units of the computer complex are integrated into a functional element. Finally, some considerations unique in a computer system of this type are described. The computer complex consists of two general-purpose, airborne digital computers and a three-section signal converter. The primary design objectives set for the computer complex were to provide 1) selective functional redundancy to enhance the probability of mission success and 2) flexibility to accommodate system mechanization changes. Redundancy has been implemented through the incorporation of backup routines in each computer and separate sections in the converter to communicate with each computer. The required flexibility has been achieved through the use of a powerful executive routine for controlling the operation of stored programs and through the allocation of provisions for additional storage and input-output.

Introduction

A GROUP of highly integrated, advanced avionic equipment is used in the Tactical Air Command F-111D airplane, manufactured by the Fort Worth Division of General Dynamics. This equipment, which carries the designation of Mark II avionics, was developed by the Autonetics Division of North American Rockwell Corporation. The Mark II avionics is comprised of an inertial navigation set, a group of sensors (attack radar, Doppler radar, etc.), a group of displays (multisensor, headup, navigation, etc.), a weapons management set, and a computer complex. A similar, less extensive group of Mark II equipment, which includes the computer complex, is also used in the Strategic Air Command FB-111A airplane.

The computer complex consists of two IBM, AN/AYK-6 (4-pi, Model CP-2) general-purpose digital computers and one Kearfott CV-2492/A programmable multiplexer/converter which serves as the interface between the computers and the rest of the avionics. The two computers are designated the General Navigation Computer (GNC) and the Weapon Delivery Computer (WDC). The GNC is primarily responsible for performing navigation-related functions, such as in-flight alignment of the inertial reference, aided-inertial navigation, route-point sequencing, airplane steering, fix-taking, fuel monitoring, data entry, and data display. The WDC is primarily responsible for performing weapon-delivery-related functions and system self-test. The converter provides all required multiplexing and data conversion for communication with the computer complex.

Computer Complex Design Objectives and Features

The computer complex has been designed to satisfy two basic criteria, i.e., failure tolerance and flexibility. These criteria were selected 1) to minimize the effects of equipment failures in the computer complex upon the operation of the avionic system and 2) to facilitate changes in system design in order to meet revised or expanded requirements.

In order to provide for failure tolerance in the computer complex, redundancy was incorporated in general at the unit level; consequently, two computers and a three-section converter capable of servicing each computer independently were selected. Only those functions deemed to be essential to mission completion (such as navigation and weapon delivery) are provided in each computer. Similarly, redundant channels are provided in the converter only for the signals associated with the essential functions. Since the successful application of this concept of redundancy depends upon failure detection, the computer complex performs comprehensive self-test and continuously monitors the characteristics of signals at the interface. When a failure is detected, switching to a backup mode in the computer complex is automatic.

In order to simplify the incorporation of mechanization changes, the computer complex has been designed 1) to operate under the control of stored programs and 2) to provide the capability for expansion of storage and input-output functions. The flexibility of a modular program organization is provided by integration of the individual subprograms through use of an executive control program. Input-output flexibility is achieved through operation of the converter under the control of stored programs. Growth provisions are available in each computer to facilitate the subsequent addition of an external storage module and an additional parallel input-output channel. The converter also contains growth provisions for additional channels of all types.

Computer Complex Functional Organization

The computer complex, represented schematically in Fig. 1, is organized along the lines of a duplex computation and conversion subsystem. Two of the three converter sections (areas I and III) provide serial digital data processing and analog-to-digital conversion for the GNC and WDC, respectively. The remaining section of the converter (area II) operates autonomously in providing digital-to-analog conversion and 28-v discrete outputs. Data to be converted in area II are selected either from area I or area III.

A selectively redundant design approach has been used in the converter. Areas I and III are essentially identical to

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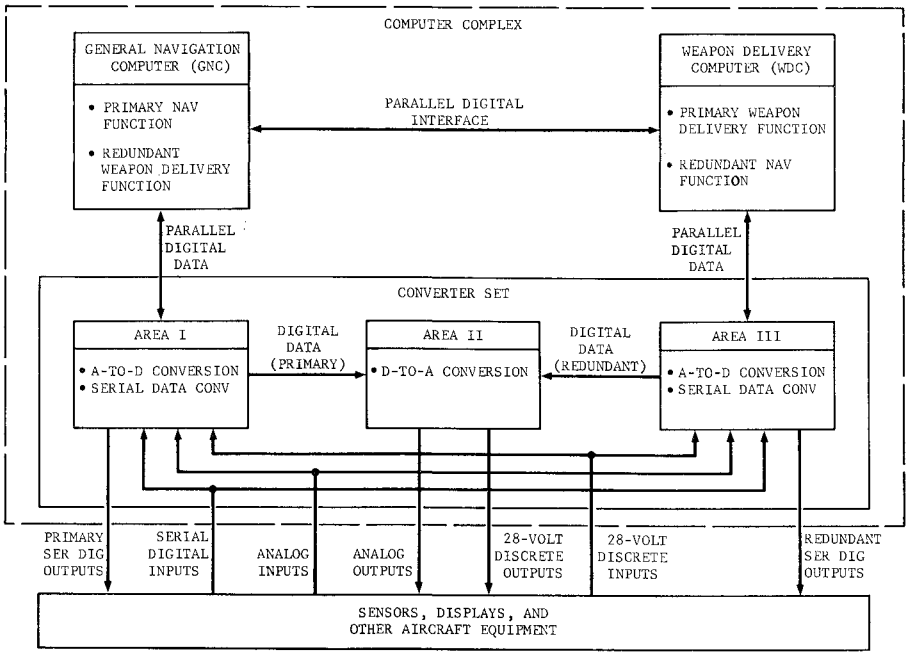

Fig. 1 F-111D computer complex functional configuration.

each other and are largely redundant. However, area II does not contain redundant outputs. This approach was selected primarily as a result of volume constraints and the necessity of interfacing with existing subsystems which were not designed to accept data from multiple sources.

In the primary mode of operation, each computer performs its respective assigned computations. All WDC outputs which are to be converted to analog form are routed to area II of the converter via the GNC and area I. The computers also periodically exchange the necessary parameters to enable either of them to take over the essential functions in the event of a failure.

Each computer and its associated area of the converter are treated as a functional unit. Consequently, a failure in a computer or in one of these areas will result in the switching of the computer complex operation into the backup mode in the operable computer and its associated converter area. For example, a failure in the GNC or in area I will result in the transfer of the computation load to the WDC and the disabling of area I. Since area II normally receives data from area I, a failure in the GNC or in area I will also result in the automatic switching of area II input circuits so that they will receive data from area III.

Table 1 Computer capability

Basic characteristics	
Formats	
Instructions	16 and 32 bit
Data	16 and 32 bit
No. instructions	61
Storage capacity	16,896 words
Stg cycle time	2.5 μsec
Index registers	1 in hardware 2 in storage
Computation performance	
Operation	Speed
Add	3.8 μsec to 10.0 μsec
Multiply	11.5 μsec to 24.4 μsec
Divide	46.3 μsec to 52.5 μsec
I/O capacity (no. channels)	
Type	Input / Output
Parallel	
Ext control	2 / 1
Prog control	... / 1
Discrete	
Control	24 / 16
Interrupt	8 / ...

Computer Description

The Mark II computer, depicted in Fig. 2, is a parallel, integrated-circuit, stored-program data processor organized specifically for use in airborne applications. It is a binary, fixed-point computer which contains destructive-readout core storage.

Computer Capability

The basic characteristics, the computational performance, and the interface capability of the computer are summarized in Table 1. The storage capacity in this table is referenced to a 16-bit word length. The variation shown in instruction execution times is a function of the instruction format length, the type of address modification used, and the data word length. The 16-bit instructions are used in most cases to conserve storage and execution time. In the case of 16-bit in-

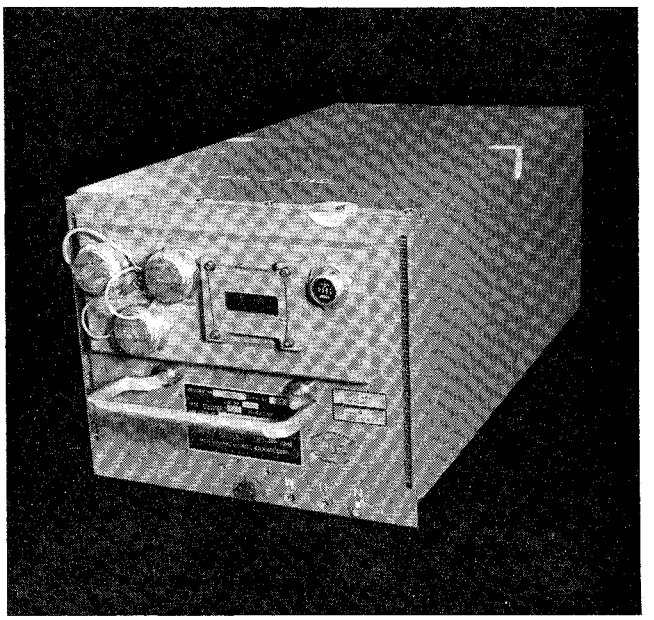

Fig. 2 AN/AYK-6 computer (IBM 4-pi, Model CP-2); 46 lb, 0.86 ft³, 2000 hr MTBF.

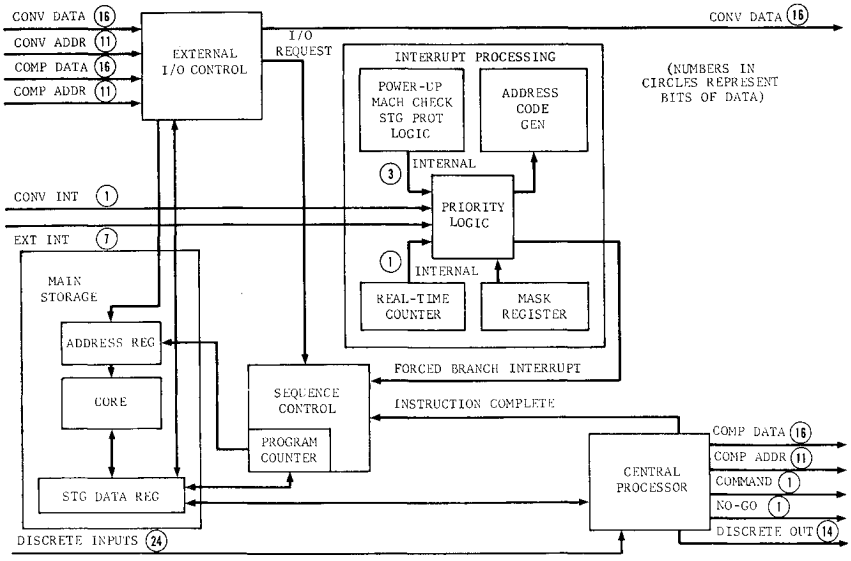

Fig. 3 Computer organization.

structions, displacement addressing is employed; the complete address is formed by the addition of the displacement to the contents of the program counter or to a base address contained in an index register. The capability of indirect addressing is also available in the computer.

Computer Functional Operation

The computer organization, presented in Fig. 3, is oriented to the performance of real-time computations with high efficiency. The significant features which enhance the real-time capability of this computer include multilevel "interrupts," a real-time counter, and provisions for external control of input-output data transfers. Features designed to provide maximum protection of stored data are also incorporated.

The interrupt system provides for fast response to priority and random stimuli. A total of twelve interrupts are available. Four of these are internal interrupts that are used to signal the detection of improper operation, real-time counter expiration, and power sequencing conditions. The remaining eight interrupts are external interrupts for use in the system application. The twelve interrupts are distributed among five different priority levels. Complete flexibility in the handling of interrupts is provided by the capability to mask interrupts under program control. Use of this feature permits selected interrupts to be temporarily ignored.

Timing signals used in effecting real-time control functions are generated through use of a real-time counter and the real-time-counter interrupt. The counter can be set and read under program control. When a specified time interval set into the real-time counter has elapsed, the interrupt is automatically generated.

The processing of interrupts is implemented by means of a sequence control. The sequence control is notified upon completion of each instruction. At this time, the sequence control checks for the existence of any pending interrupts that can be processed. An interrupt cannot be processed if it is masked or if it is held as the result of the processing of another interrupt of the same or a higher priority level. When an interrupt is accepted, sequential instruction processing is preempted, i.e., the contents of the program counter are stored, and the next instruction is obtained from an address specified by the interrupt processing logic.

Through use of the externally controlled input-output section, high-speed input-output data are transferred directly to and from the storage unit without alteration of the program flow. Whenever an input-output request from an externally controlled channel is presented, access to storage for the processing of the input-output word is automatically interleaved with access to storage by the central processor. Computation is suspended for one storage cycle while the input-output word is transferred into or out of storage.

Special precautions are taken to prevent inadvertent loss of the contents of the destructive-readout core storage. Each storage word contains a storage-protection bit, which can be changed only through use of aerospace ground equipment, to designate words that must not be altered under program control. If the storage unit receives a clear/write command for one of these words, a storage-protection interrupt will be activated. Further protection is afforded through the storage of a parity bit with each word and through the checking of parity before any word is transferred out of the storage unit. In addition, if the computer input power drops below a design threshold voltage, the regulated power supplies are deactivated in a controlled sequence. This orderly deactivation inhibits possible alteration of the contents of computer storage as a result of power supply transients.

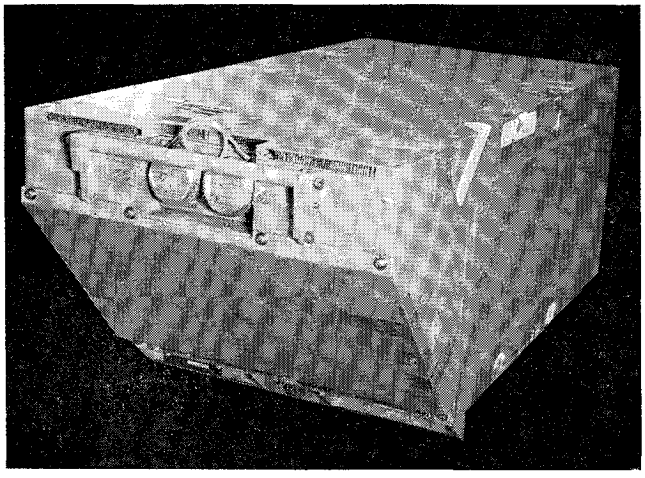

Fig. 4 CV-2492/A multiplexer/converter (Kearfott); 49 lb, 0.89 ft³, 1500 hr MTBF.

Converter Description

The Mark II multiplexer/converter, depicted in Fig. 4, is a programmable, solid-state data conversion unit designed specifically to Mark II requirements. Its major functions are to convert and multiplex the data used in communication between the computer complex and other equipment. The converter is capable of processing serial digital, analog, and discrete signals. Data are transmitted between each computer and its respective area of the converter over a separate two-way parallel digital channel. These 16-bit channels are

Table 2 Converter capability

Conversion performance		
Type	Resolution	Accuracy
d.c.	12 bits + sign	0.033%
a.c.	12 bits + sign	0.04%
Synchro	14 bits	3 min

I/O capacity (no. channels)		
Type	Input	Output
Analog		
d.c.	9	12
a.c.	2	2
Synchro and resolver	16	7
Discrete		
28-v d.c.	14	19
5-v d.c.	...	14
Digital		
Serial	21	16
Parallel	2	2

operated under the control of the converter. A separate converter program is used to control the operation of each of the two areas which communicate directly with the computers. Converter program instructions are stored in the computers and are brought to the converter, as needed, via the 16-bit channels.

Converter Capability

The capability of the converter is summarized in Table 2. The converter makes use of 23 instructions which control the conversion of data and the selection of converter program sequences. To provide for high data rates in the execution of instructions, certain time-consuming functions are performed off-line. These functions include the sampling and conversion of synchro and a.c. inputs (in a time span of 1.25 msec) and the input or output of serial data (in a time span of nominally 260 μsec per word).

Information is processed in the converter on the basis of a frame time of nominally 320 μsec. In each frame time, there are 212 μsec available for the execution of instructions. The remaining time is reserved for the processing of serial input-output data. One serial input or output word can be processed in each frame time. Maximum times required for the execution of other conversion instructions are summarized in Table 3; these times are based on the assumption that there are no conflicting functions which introduce delays. Delays may result from 1) the sequential execution of functions that are implemented through the use of shared equipment, such as the analog-to-digital converter, or 2) an interruption which occurs at the completion of the off-line portion of a synchro or a.c. input function to permit the data to be transmitted to the computer.

Table 3 Converter instruction execution times

Type	Input	Output
d.c. voltage	212 μsec	54 μsec
a.c. voltage, synchro	31 μsec[a]	54 μsec
28-v discrete	54 μsec	54 μsec

[a] Off-line sampling.

Converter Functional Operation

The three separate functional areas of the converter are shown in Fig. 5. Input-output data processing is performed in each of the autonomous input and control areas that serve the GNC and WDC (areas I and III, respectively) under the control of converter instructions. These instructions are stored in the computers and are carried out by the program execution logic in the converter. In addition to the program control functions provided in areas I and III, analog inputs, 5-v discrete inputs, and serial digital inputs are converted to parallel digital form, and parallel outputs are converted to serial digital form. The serial data processing includes the detection of errors in serial inputs by means of parity, built-in test, synchronization pulse count, and gap-time monitoring. In order to provide completely autonomous operation, areas I and III each contain their own power supplies.

Converter instructions are used to provide for the processing and conversion of computer complex inputs and outputs, the sequencing of converter instructions, and ancillary functions

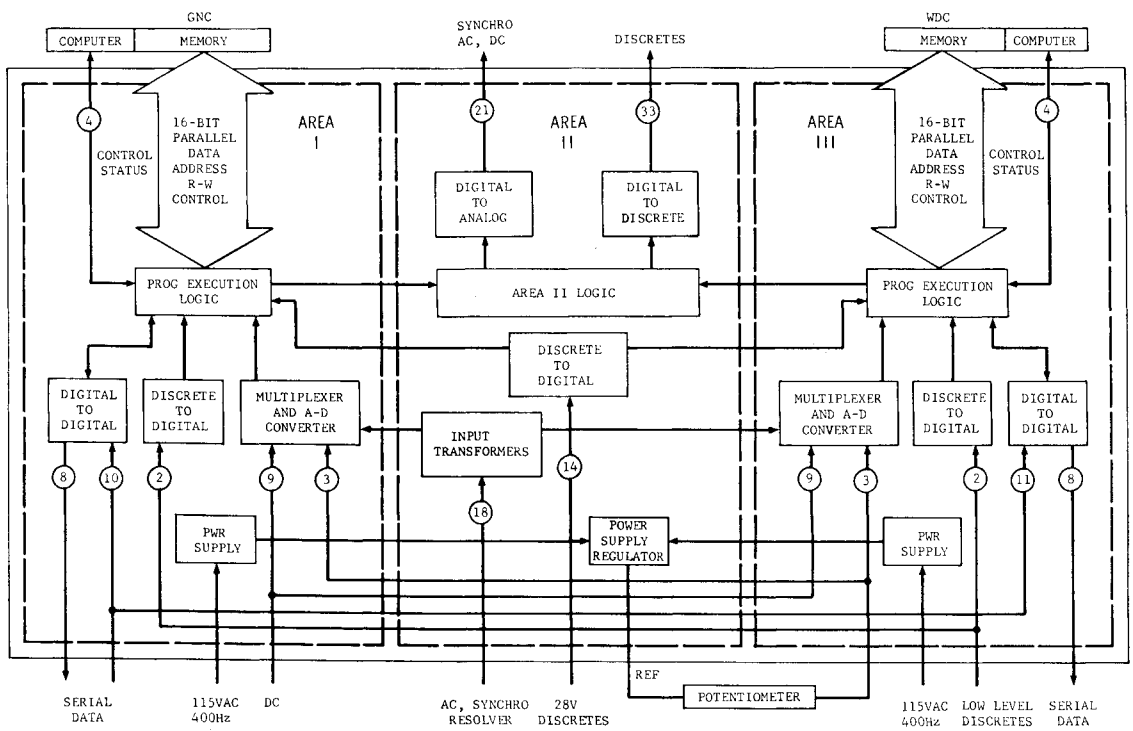

Fig. 5 Converter organization.

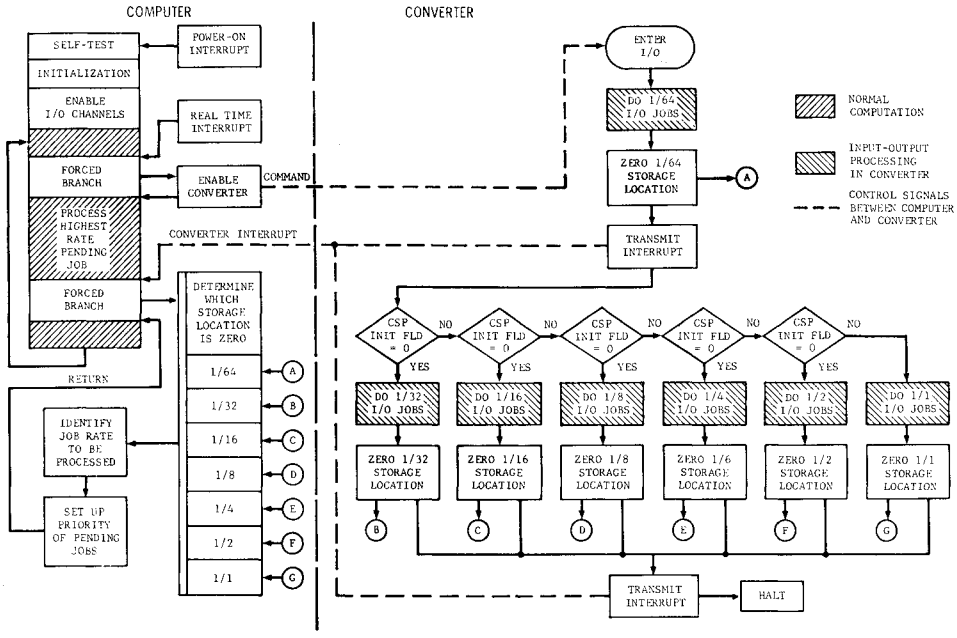

Fig. 6 Computer/converter program interface.

related to communication with the computer. Consecutive converter instructions are normally obtained from consecutive addresses in the computer. However, the normal instruction sequencing can be altered through use of "conditional skip" and "unconditional transfer" instructions. Ancillary instructions include one which transmits a zero value to a specified storage location in the computer, one which causes the converter to halt, and one which causes the converter to send an interrupt to the computer.

Digital-to-analog conversions and digital-to-28-v discrete conversions are performed in area II under the control of either area I or area III. Area II also contains nonredundant Scott-T and isolation transformers for synchro, a.c., and resolver inputs. (Redundancy is not used for two reasons: the inherent reliability of the transformers is high, and the weight and volume constraints make such redundancy infeasible.) In addition to the nonredundant transformers, reference voltage generation and the conditioning of 28-v discrete inputs are provided in nonredundant fashion in area II. Area II may obtain unregulated d.c. power from either area I or area III.

The computer participates extensively in the self-test of the converter. Stored values obtained from the computer are converted first to analog form, then converted back into digital form, and finally sent to the computer. The computer compares the doubly converted data with the stored values and uses the differences to determine whether a go or no-go condition exists.

Computer Complex Operation

The operation of the computer complex is effected under the control of the executive routine in each computer. This routine serves as a master control program for each computer and its associated area of the converter. As a result of the periodicity requirements for the computation and the transmission of input-output parameters, the executive routine is used to schedule computations on the basis of required rates. The assignment of subprogram and parameter rates is determined as a function of over-all system needs. Seven different processing rates have been established for the F-111D system, and the various functional subprograms and input-output parameters are grouped in accordance with the proper rates.

The resulting groups of subprograms and input-output parameters are called rate groups. The executive philosophy is such that the input-output processing for each rate group is initiated at the proper time through the use of the real-time counter and its associated interrupt. The input-output processing is then effected in the converter under converter program control. Upon completion of the input-output processing of the rate group, the converter notifies the computer so that the computations required for that rate group can be scheduled. Scheduling is such that the order of priority is determined on the basis of the computation rates of the functional subprograms to be executed. The relationship between the processing which takes place in the computer and the converter and the operation of the executive routine are described in the following paragraphs.

Converter Program Operation

The converter program is subdivided into sections in accordance with input-output (I/O) rates. In the F-111D computer complex, the possible rates range from once per sec to 64 times per sec in steps which are power of two, i.e., 2, 4, 8, 16, and 32 times per sec. Each second is subdivided into 64 equal intervals, and in general, the inputs and outputs of the 64-per-sec rate group and one other rate group are processed in each of these intervals.

The relationships between the converter program and the computer program are illustrated in Fig. 6. Converter program control is maintained in the computer executive routine through the processing of interrupts. When power is first applied, input-output processing is inhibited until self-test and initialization of the computer are completed. Interrupts from the real-time counter every $\frac{1}{64}$ sec provide timing for the initiation of converter input-output sequences. When a real-time interrupt occurs, the computer sends a "command" pulse to the converter to initiate instruction accessing.

The 64-per-sec rate group is always processed first. When the processing of this group has been completed, the converter 1) sends a zero to a computer address that represents the status of the 64-per-sec rate group, 2) transmits an interrupt to the computer, and 3) starts searching for the next rate group to be processed. This searching is effected through the use of "conditional skip" (CSP) instructions. Each execution of a CSP instruction results in decrementing a specified field of the instruction word by one and testing the contents of the field for a zero value.

The identification of a zero value leads directly to the processing of inputs and outputs of a particular rate group. If a zero is not found, access is provided to the next instruction in sequence (this instruction is usually an unconditional transfer to another CSP instruction associated with another

rate group). In each case, when the processing of a rate group has been completed, the converter sends a zero to a storage location used to identify the completed rate group and transmits an interrupt prior to processing the next instruction.

The converter interrupt is used to inform the computer executive routine that the transmission of a particular rate group of input-output data has been completed. The executive routine identifies the input-output rate group which has been processed and establishes the functional subprograms which must be executed in order to generate new outputs for that rate group. The executive routine also establishes the priorities of subprograms used in setting up the queue sequence needed to interleave the computations required for a given rate group with the transmission of input-output parameters of that group.

Executive Control

The executive control routine is primarily a real-time queuing routine which functions as an operating system to integrate the various subprograms into the flight program. The executive routine consists of several interrelated subroutines which provide data transmission, mode analysis, real-time control, and interrupt processing. All functional subprograms (jobs) are processed under executive control. The GNC and WDC executive routine mechanizations are essentially the same with the exception of condition, job, and other data tables used to control the subprograms assigned to each computer.

Operation of the executive routine is summarized in Fig. 7. The real-time clock interrupt, converter processing, and converter interrupt portions of the executive routine have been described in conjunction with the operation of the converter program. The control of the executive routine over the flight program is effected primarily through 1) the mode analysis subroutine, which is used to select the proper subprograms to be executed to implement the current avionic system operating mode and 2) the real-time control subroutine, which is used to establish the relative priorities for execution of the functional subprograms. Tasks which cannot be handled on a periodic, scheduled basis or involve critical timing are processed through use of interrupts. These interrupts preempt the scheduling established during the execution of the real-time control subroutine.

The mode analysis subroutine is used to establish the program flow criteria through use of system condition words. Each condition word represents a collection of the current positions of panel switches and equipment status information which is used to determine whether to employ a given system operating mode. In the mode analysis subroutine, condition words are formed and compared with criteria for the selection of the possible system modes. These criteria are permanently stored in decision tables. Equality between a condition word configuration and a set of criteria in the decision table is used to activate the necessary subprograms to perform the indicated function or mode.

The real-time control subroutine is used to maintain the execution status of each subprogram and to select the highest priority subprogram for execution upon completion of the processing of each subprogram or converter interrupt. Each time the real-time control subroutine is used, the highest priority subprogram is determined on the basis of the computation rates of the subprograms remaining to be executed. Additions are made to the subprograms to be executed as a direct consequence of a converter interrupt. As each functional subprogram is executed, its status indicator is changed accordingly. The real-time control subroutine is used to set up the proper entry condition (initial or normal) of each subprogram and to transfer control to that point when that subprogram is to be executed. Upon the completion of execution of each subprogram, control is returned to the real-time

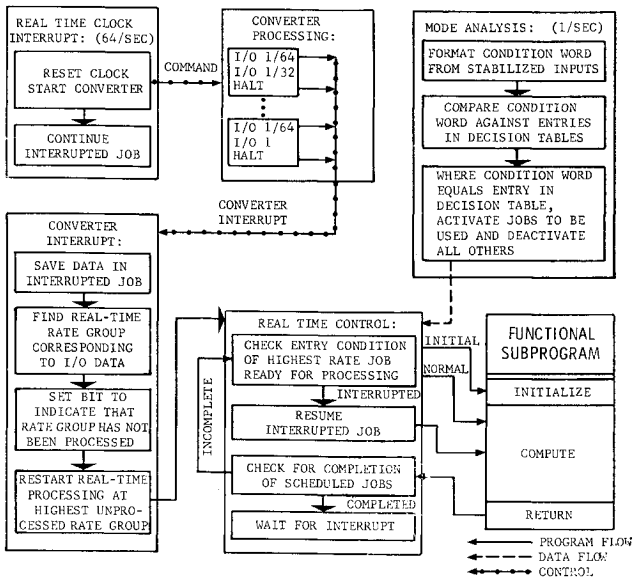

Fig. 7 Executive routine structure.

control subroutine. Entry and exit from the mode analysis subroutine are also handled in this manner.

In the processing of interrupts, the contents of active registers are first stored to permit future resumption of the interrupted subprogram. When the computations required as a consequence of the interrupt have been completed, the contents of all active registers are restored, and normal computation is resumed.

Specialized Considerations in Multicomputer Systems

The use of a multicomputer system is such that special consideration must be given to the factors which are unique in the operation of this type of system. The major considerations involve the detection of malfunctions, the specification of the criteria for switching of operation, the mechanization of the switching, the handling of computation transients during switching, and the distinction between power-off and malfunction conditions. Other considerations involve the extent of the redundancy to be provided and the selection of redundant functions. The increased number of interconnections among equipment that results from the use of a multicomputer configuration can also be very significant.

Special attention must be paid to the relative physical placement of the units of the computer complex in the airplane equipment bay because of the large number of interconnecting wires and the relatively high-speed operation of parallel data transfer channels. As an example of the significance of this type of interface, the parallel channels within the F-111D computer complex contain 320 wires. Cable runs of this size must be kept as short as possible in order to minimize weight and susceptibility to noise. Therefore, the two F-111D computers and the converter are mounted in one equipment rack which contains all wiring and EMI shielding for each parallel channel.

Consideration must also be given to the possibility that power may not be available for all parts of the system, such as a computer or an area of the converter. Provisions must be made to prevent a unit without power from affecting the proper operation of other units. The data transfer control receiver circuits must be designed so that acceptance of data is inhibited when the transmitting unit is turned off. In addition, data transmission must be inhibited during equipment turn-on and turn-off.

Careful consideration must also be given to the effects of delays in activating redundant backup computations whenever this mode of operation becomes necessary. When a real-time

solution, such as the computation of weapon-delivery release time, is in progress and a malfunction results in the switching of operation to the other computer, any delay could affect overall system performance. When redundant modes remain dormant and are activated only when the primary mode is inoperable, transients caused by switching will occur in some mode mechanizations. These transients can be minimized by continuous operation of affected redundant modes. Since weapon delivery accuracy is of utmost importance, the weapon delivery equations are solved simultaneously in both F-111D computers.

There are other factors which cause the programming task and the total storage utilization to increase as a result of the use of two computers. These are:

1) Self-test. A very efficient self-test program must be implemented in order to detect failures in flight so that the switching of operation can be controlled.

2) Communication. The computers must communicate with each other; consequently, additional programming and input-output operations are required.

3) Duplication. There are certain functions, such as executive programs and mathematical subroutines, that must be duplicated in each computer.

The end result is that two computers do not provide twice the performance of one when they are operated in a dual computer configuration, such as the F-111D computer complex. Therefore, allowance for this factor must be made in the determination of individual computer performance requirements.

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Thunderstorm Turbulence and Its Relationship to Weather Radar Echoes

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Measurements of turbulence intensity made during 100 penetrations of storms in Oklahoma by instrumented aircraft, at altitudes between 23,000 ft and 37,000 ft, have been compared with properties of the weather radar echoes from the storms. The frequency of encounters with moderate and severe turbulence increased markedly with the maximum radar reflectivity of the storm. The frequency of severe turbulence encounters was greater during penetrations that passed through storm cores than during those that missed the cores by five miles or more, and somewhat greater near 25,000 than at 35,000 ft. The aeronautical implications of the study and the extrapolation of results to storms in other parts of the world are discussed.

1. Introduction

THUNDERSTORMS have been a severe hazard to aircraft throughout the history of flying. The hazards of hail and turbulence in relation to flight were first documented systematically during the Thunderstorm Project of 1946–47[1,2]; later, United Air Lines conducted important studies in conjunction with commercial flights over midwestern United States during the 1950's.[3] The problem has been highlighted by accidents and incidents involving jet transports,[4] and it appears that flight through thunderstorms is best avoided by transport-type aircraft. The economics of civil aviation operations demand that disruption of normal services be minimized, however, while a satisfactory level of safety is maintained.

In an attempt to increase understanding of thunderstorm turbulence in relation to aircraft design and the planning of safe flight operations in a stormy atmosphere, a team of scientists from the Royal Aircraft Establishment spent six weeks during May and June 1965, in Oklahoma, working in collaboration with scientists from the U.S. National Severe Storms Laboratory, Norman, Oklahoma. This paper reports on one aspect of this cooperative program, which has been partially documented elsewhere,[5] and extends other earlier studies.[6–9]

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2. The Test Aircraft and Their Instrumentation

The test aircraft discussed here were an F100F of the Aeronautical Systems Division, USAFSC, Wright Patterson AFB, Dayton, Ohio, and a Scimitar F1 of the Royal Aircraft Establishment, Bedford, England. These swept-wing transonic fighters have similar dynamic characteristics at the speeds and altitudes used in the tests. Parameters recorded continuously on galvanometer oscillographs included the acceleration of the center of gravity normal to the aircraft axes, the airspeed, and the barometric height. The frequency response of the accelerometer channels on the two aircraft was similar and covered the rigid body and first few aeroelastic modes.

3. Ground-Based Radars

The primary meteorological radar was the WSR-57 of the National Severe Storms Laboratory (NSSL). This radiates a 10-cm wavelength and is equipped with both a step attenuation program and a contoured echo intensity presentation[10] (Fig. 1). The measure of the strength of radar echoes used